



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,997	07/08/2003	Dennis Harold Burke JR.	TI-34951	8166
23494	7590	01/06/2009		
TEXAS INSTRUMENTS INCORPORATED				
P O BOX 655474, M/S 3999				
DALLAS, TX 75265				
EXAMINER				
CHUNG, PHUNG M				
ART UNIT		PAPER NUMBER		
2117				
NOTIFICATION DATE		DELIVERY MODE		
01/06/2009		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

### Office Action Summary

**Application No.**

10/614,997

**Applicant(s)**

BURKE ET AL.

**Examiner**

PHUNG MY CHUNG

**Art Unit**

2117

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10/2/08.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-13, 16, 17 and 21-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-13, 16-17 and 21-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SI-08)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_
- Paper No(s)/Mail Date \_\_\_\_\_

**DETAILED ACTION**

1. The indicated allowability of claims 2-13, 16-17 AND 21-24 is now withdrawn.

Rejections as follow.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-13, 16-17 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant admitted prior art (hereafter referred to as the AAPA, (Us 2005/0010842 A1)) in view of Chun et al (US 2003/0154047).

As per claims 2-5, the AAPA discloses a method of testing at least one mixed signal semiconductor device (col. 1, paragraph (0002)), the method comprising: when a test program is executed in a tester user interface environment, the test program sets up the test specific hardware modules in a device tester unit and executes the tests. Once the test program is initiated, the tester user interface transfer the control of tester unit to the test program and the control is not returned back to the tester user interface until the test program completes the test execution. Typically, the test program sets hardware modules in the device tester unit for a first test, executes the first test, performs appropriate computations on the data collected by the first test, evaluates the results of the first test and then sets the hardware modules for the next test (col. 3, paragraph (0021) lines 9-23). These steps are performed serially, but not in parallel. It

would have been a matter of design choice to a person of ordinary skill in the computer art to program the test in serial or in parallel (0026) as desired when needed. However, Chun et al disclose that a tester for the mixed signal semiconductor device should have a special structure in which analog signals and digital signals are simultaneously handled. (See paragraph (0006)). Therefore, a person of ordinary skill in the computer test art, at the time the invention was made, to incorporate the tester for the mixed signal semiconductor device should have a special structure in which analog signals and digital signals are simultaneously handled as taught by Chun et al into the test program of the AAPA so that the serial test can be reprogram to perform the test for the mixed signal in parallel so that the next test (the second test) can be executed concurrently with the processing of the test data resulting from the first test to reduce test time.

As per claims 6-7 and 9, the teaching of the AAPA and Chun et al have been discussed above. They do not specifically disclose that the first and second test are configured in an interpreted software language is Interactive Test Pascal. However, it would have been obvious design choice to a person of ordinary skill in the computer art to use the first and second test in interactive test Pascal or other software language as design when needed.

As per claims 8 and 10-11, the teaching of the AAPA and Chun et al have been discussed above. They do not specifically disclose storing the first test result and/or second test results in a first and/or second information storage or in a single storage unit. However, it would have been obvious to a person of ordinary skill in the test art, at

the time the invention was made, to store the first test result and/or second test results in a first and/or second information storage or in a single storage unit for later use or repair when needed.

As per claims 12-13 and 16-17, these claims are rejected under similar rationale as set forth in claims 2-5.

As per claims 21 and 23-24, these claims are rejected under similar rationale as set forth in claims 8 and 10-11.

As per claim 22, this claim is rejected under similar rationale as set forth in claims 6-7 and 9.

4. Applicant's arguments with respect to claims 2-13, 16-17 and 21-24 have been considered but are moot in view of the new ground(s) of rejection.
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is (571)272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phung My Chung/  
Primary Examiner  
Art Unit 2117